National Aeronautics and Space Administration

Burn-in of Microcircuits

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The Rover Environmental Monitoring Station (REMS) on NASA's Curiosity Mars rover includes temperature and humidity sensors mounted on the rover's mast. One of the REMS booms extends to the left from the mast in this view.
Image credit: NASA/JPL-Caltech/MSSS

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Abstract

Burn-in (BI) is the key screening step for electronic components. It is performed to reduce product infant mortality by weeding out parts susceptible to early failure. Our recent audit and specification work has shown that the microcircuits burn-in screening requirements as stated in MIL-STD-883, Test Method 5004, are out of date and can have multiple interpretations. At the request of NASA, the Aerospace Corporation, and other concerned organizations, a JC13 Task Group was formed to provide guidance. This paper will describe the issues and provide a status update on microcircuit burn-ins. This work was performed for NEPAG, the NASA Electronic Parts Assurance Group.

Microcircuits Burn-in (BI) Screening Requirements Are out of Date and Have Multiple Interpretations

- **BI is the key screening step** – considered necessary to weed out product infant mortality.
- Our recent audit and specification review work has shown that the microcircuits BI screening requirements as stated in MIL-STD-883, Test Method 5004, are **out of date and have multiple interpretations**.

- **Why are they out of date?**
  - Were developed more than 25 years ago
  - Then: were at 5-micron technology node
  - Now: 45-nm space products are on their way to QMLV qualification (Ref: Lew Cohn's talk on Tuesday). Made possible by
    - Dual use technology
    - Advances in packaging technology
    - Availability of system-on-a-chip (SOC) products, which could be easily called assemblies
  - With column grid arrays (CGAs), reached limitation for complete screening.
  - Changing business landscape

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Microcircuits Burn-in (BI) Screening Requirements Are out of Date and Have Multiple Interpretations (Cont'd)

- **No clear interpretation** any longer
  - Varied implementation
- **Periodic, frequent updates are needed!**

- **Recent Activities**
  - At the request of NASA, the Aerospace Corporation and others, a new JC13 Task Group was formed to provide guidance.
  - More rigorous assessment done during audits and specification reviews.

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Findings from Microcircuit Audits & New Technology Data Reviews

Supplier audits. The audit team reviews screening travelers and burn-in circuits (Done on one or two typical products used on space programs). Some of the findings were:

- **Disabled chip burn-ins.** Recent audit for QML device discovered that a chip was disabled during static burn-in; thus, it was not drawing any current.
  Recommendation: For new SMDs, add a statement within burn-in paragraphs stating that parts shall be kept in their enabled state during burn-in.
- **Class Q 160-hr/125ºC burn-in.** Interpreted as static burn-in.
  Recommendation: Provide specific guidelines in MIL-STD-883, Test Method 5004.
- **At-frequency (dynamic) burn-ins.** Test equipment limitation cited for not doing burn-ins at application frequency.
  Recommendation: Burn-in task group to discuss and provide guidance. When SMD says that a part can be used at 200 MHz, doing burn-in at 6 MHz (cited as "burn-in equipment limitation frequency") is not meaningful!
- **Two static burn-ins.** Some manufacturers do electrical testing between two static burn-ins, whereas others do electricals after completing both static burn-ins.
  Recommendation: Provide specific guidelines in MIL-STD-883, Test Method 5004.
- **Thermal imaging.** For a device with hot spots, thermal resistance, junction-to-case would be much higher than guidelines given in MIL-STD-1835. One supplier used thermal imaging to find hot spots on the die.
  Recommendation: Assign a task group to evaluate effectiveness of thermal imaging at product development stage.

NASA Inputs to BI Task Group

1. **Clarify burn-in requirements** for space products in Table I of Method 5004: specifically, screening steps 3.1.10, 3.1.12, footnote 9/, and footnote 10/. As written, it implies that dynamic burn-in is a requirement. However, this is not always done. Moreover, for certain functions, such as a precision voltage reference, how would you design a dynamic burn-in? Requirements need to be reviewed and updated.

2. **High-temperature reverse bias (HTRB) vs. static burn-in**. Table I of Method 5004 has no mention of static burn-in. We all know that digital products are subjected to static burn-ins, often two: one for low condition (Static I) and the other for high condition (Static II). Add reference to static burn-in(s) as appropriate.

3. **How are burn-in voltage, frequency, etc. supposed to be determined?**

4. **Are any manufacturers using low temperature burn-in?** If yes, a low-temp burn-in option should be included in the screening spec.

5. **What activation energy (Ea) should be used for new technology?**
   Some manufacturers are using a fixed Ea of 0.7 eV.

6. **Time-temperature regression tables (e.g., Table I in Method 1015) should be reviewed.**
   What Ea are they based on? Is that Ea still valid?

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NASA Inputs to BI Task Group (Cont'd)

7. Limited-temperature parts:

- Anything not meeting full MIL temperature range (–55ºC to +125ºC)
- If the part rating has a maximum temperature less than +125ºC, what is the temperature and duration of the burn-in?

8. Dynamic burn-in for high-speed devices.

- What frequency should be used?

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Additional NASA Inputs to JC13 Task Group
Static Burn-in Circuits

- **Considerable variation on how they are implemented.**
  - **Single circuit used with half of the inputs biased low and the other half biased high.**
    - Post static burn-in electricals done.
  - **Two Circuits used.**
    - All inputs low (Static I)
    - All inputs high (Static II)
    - Post static burn-in electricals done **after completion of both** (Static I and Static II) burn-ins.
  - **Two circuits used.**
    - All inputs low (Static I)
    - All inputs high (Static II)
    - Post static burn-in electricals done **after completion of each** static burn-in.
  - **Task Group review and guidance requested. Also, clarify which inputs are being used and their settings: data, control, address, clock,…?**

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Task Group – 2011-01
SMD Electrical and Burn-in Guidelines

- Charter for Task Group. Develop JEDEC document for guidance to suppliers and users that includes recommendations on Deltas, SMD electrical parameters, and Burn-in. Also, provide recommendations for any needed changes to MIL-STD-883.

1. Burn-In
    a. types required - dynamic and static/high-temperature reverse-bias burn-in (HTRB)
    b. burn-in specified by technology or product type
    c. junction temperatures to be achieved
    d. burn-in conditions - voltages, frequency, etc.

2. Delta Requirements
    a. definition - critical parameters selected to provide a measure of product and process stability
    b. selection of delta parameters

3. Electrical Measurements
    a. parametrics
    b. functional
    c. selection of limits based on what?
    d. parameters guaranteed
        1) but not tested
        2) by design
        3) by characterization data
        4) data required to validate guaranteed position

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New JEDEC Document

- **In draft form, expected release September 2015**
- **Title: Selection of burn-in/life test conditions and critical parameters for QML microcircuits**
- **The document covers**
  - Terms and definitions
  - Burn-in stress and electrical test conditions development
  - Burn-in conditions evaluations
  - Burn-in and electrical measurements
- **Will be a guideline document**
- **The Task Group will remain open to address the remaining issues**

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Issues Going Forward

- **Alternate methods for deep submicron technologies**
  - Wafer level burn-in, others
- **Limited-temperature (restricted-temperature) range parts**
  - BI temperature
  - BI duration – time/temp table in TM 1015, applies to hybrids but is not applicable to monolithic microcircuits
  - What temp range to do final (post BI) electricals
- **New technology - CGAs**
  - Suppliers don't recommend post-CGA BI
  - How to ensure infant mortality removal after installation of columns
- **Low leakage currents and their delta limits**
- **Burn-in of high-speed parts**
- **Hybrids parts**
  - BI temperature, time, voltage
  - Element evaluation burn-in
- **Hybrid crystal oscillators**
  - BI temperature, time, voltage
- **Any other issues as they arise**

Dual Use Technology

- Basically an infusion of commercial monolithic microcircuits into DoD system.
  - Rad hard by design 45nm CMOS microelectronics technology (BAE Systems, built at IBM foundry)
  - Adding their unique processing steps to the existing processes, e.g. MRAMs being offered by Aeroflex and Honeywell (done in collaboration with Everspin)
  - Upscreening selected products from commercial portfolio (Analog Devices)

- This has resulted in paradigm changes. An example follows:
  - Not all parts are specified over the full military temperature range, –55°C to +125°C. Many of them are specified over –40°C to +110°C operating temperature range. These differences are now clearly shown in the standard microcircuit drawings (SMDs). However, there are **no** guidelines for BI of these devices. (Per notes 3/ and 4/ of the regression table, doing BI at temperatures lower than 125°C is not allowed for monolithic microcircuits.)

MIL-STD-883J
w/CHANGE 1

TABLE I. Burn-in time-temperature regression. 1/ 2/ 3/ 4/

Minimum temperature T_A (°C)	Minimum time (hours)			Test condition (see 3.1)	Minimum reburn-in time (hours)
	Class level S	Class level B	Class level S hybrids (Class K)		
100	—	352	700	Hybrids only	24
105	—	300	600	"	24
110	—	260	520	"	24
115	—	220	440	"	24
120	—	180	360	"	24
125	240	160	320	A - E	24
130	208	138	—	"	21
135	180	120	—	"	18
140	160	105	—	"	16
145	140	92	—	"	14
150	120	80	—	"	12
175	—	48	—	F	12
200	—	28	—	"	12
225	—	16	—	"	12
250	—	12	—	"	12

1/ Test condition F shall be authorized prior to use and consists of temperatures 175°C and higher.
2/ For condition F the maximum junction temperature is unlimited and care shall be taken to ensure the device(s) does not go into thermal runaway.
3/ The only allowed conditions are as stated above.
4/ Test temperatures below 125°C may be used for hybrid circuits only.

METHOD 1015.10
26 February 2010

Signal Integrity Capacitors

- **Signal integrity capacitors used in microcircuits**
  - MIL-PRF-38535, Para 3.15.1 specifies screening requirements.
  - Base metal electrode (BME) capacitors used with low-voltage high speed microcircuits do not meet Para 3.15.1.
    - BMEs were meant to be used in commercial applications.
    - However, the upscreened versions of the BMEs have also found their way into microcircuits and hybrids of interest to the space community.
    - The suitability of BMEs for use in space applications is being evaluated by
      - JEDEC, G12, NASA, Aerospace, ESA, and JAXA.
    - The goal is to have an acceptable screening flow this fiscal year. (MIL-PRF-THIN and associated slash sheets)
    - It should be noted that these screened BME capacitors would see additional screening including the burn-in(s) at the unit level.

Other Updates on Microcircuits

- **Class Y**
  - A new class created for complex ceramic based non-hermetic microcircuits
  - Introduced PIDTP (Package Integrity Demonstration Test Plan)
  - MIL-PRF-38535K (the latest revision) includes requirements for Class Y.
  - Front-runner suppliers: Xilinx, Honeywell, Cobham/Aeroflex, e2v
  - Currently addressing testing of underfill and thermal interface material (TIM) adhesive to meet the requirements of MIL-STD-883, Test Method 5011.
  - Manufacturers have the requirements; we will see what works and what needs changing in actual practice.
- **Signal Integrity Capacitors**
  - Slash sheets for InterDigitated Capacitors (IDCs) used in Xilinx V-5 FPGAs are yet to be developed.
- **PEMs Upscreening Flows**
  - Flows developed for terrestrial and space applications
- **Bond wires used in plastic encapsulated microcircuits (PEMs)**
  - New industry effort started for copper bond wires – weekly telecons
- **JC13.7 Task Group**
  - New electronic device technology trends
  - Trying to get standards in front of technology.
- **Refer to JEDEC/G12 websites for details**

Thank you!

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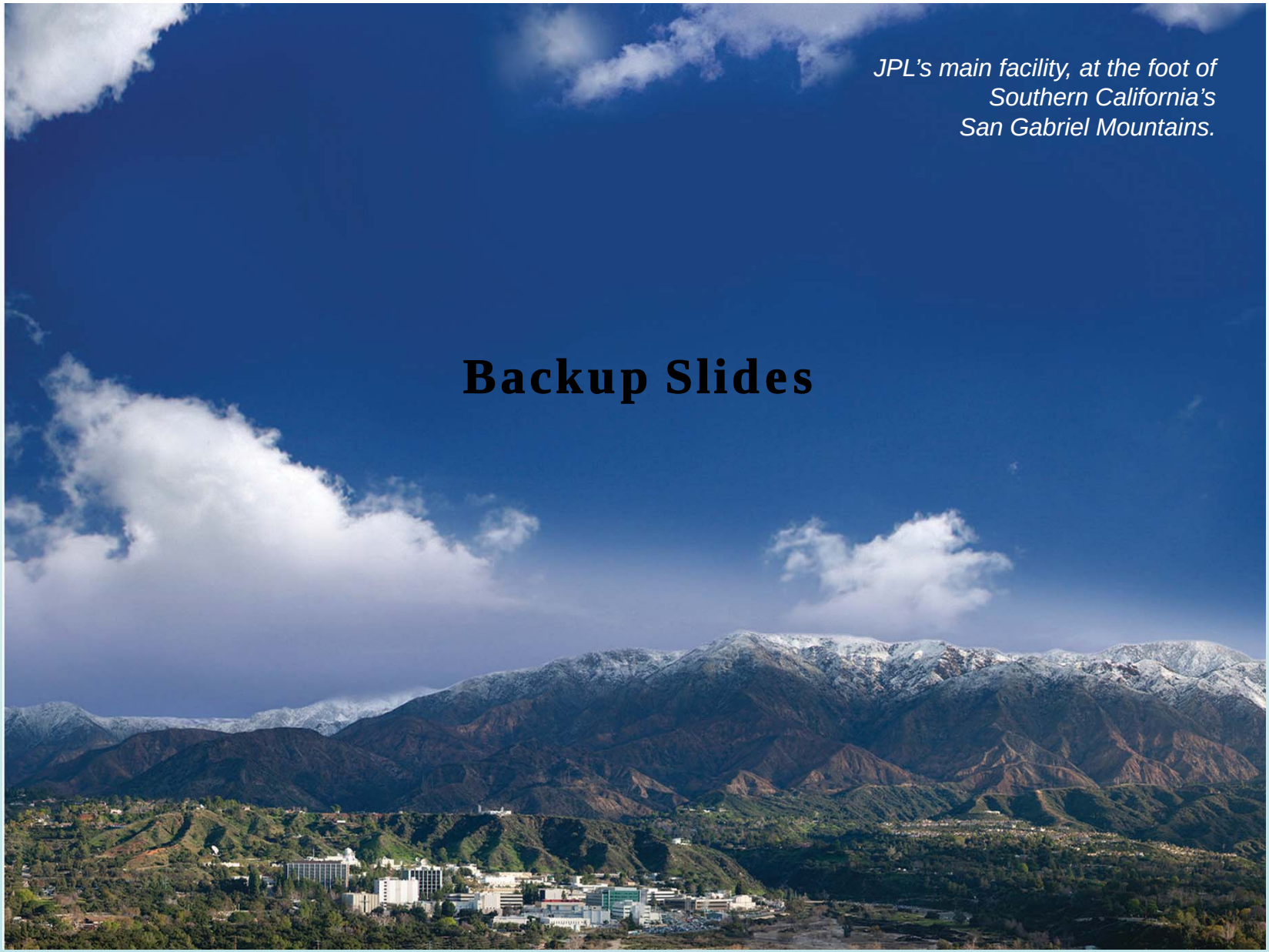
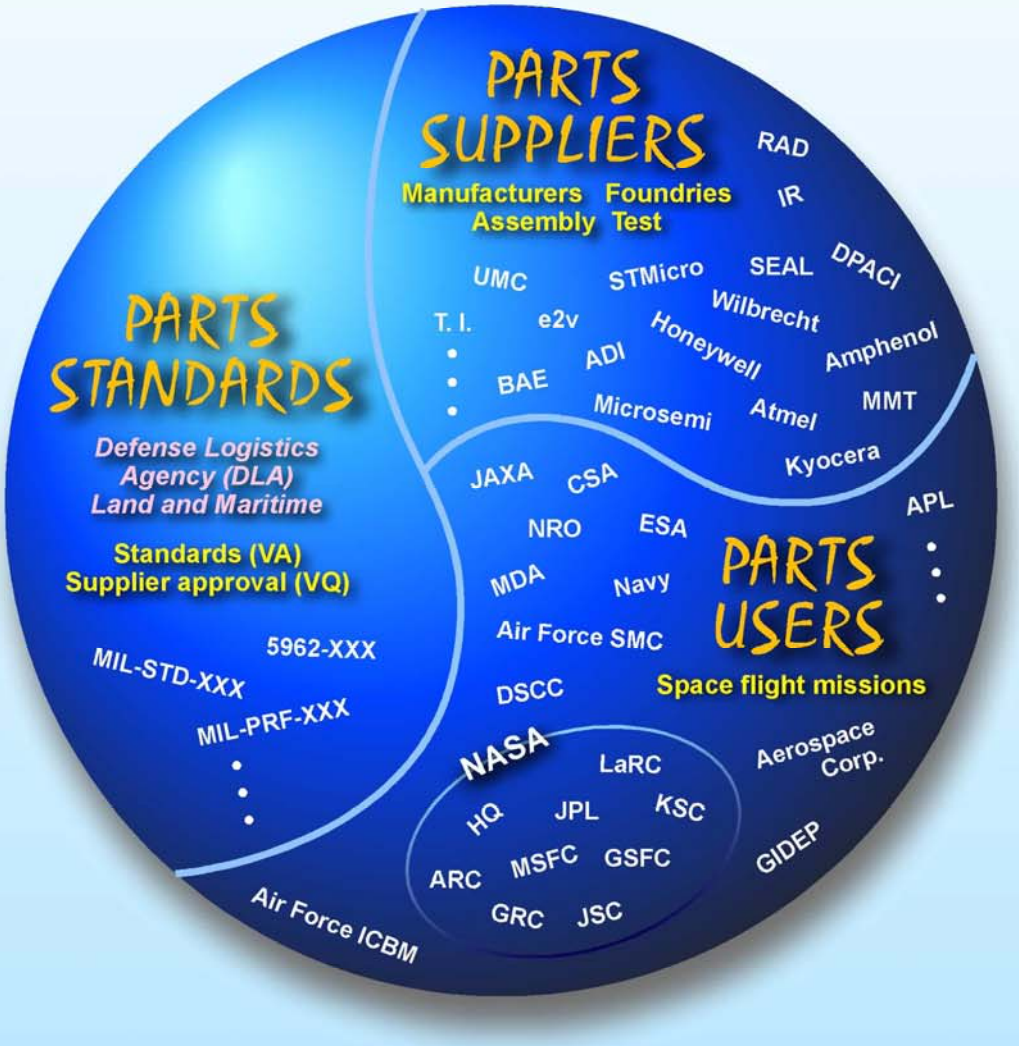


Backup Slides

Space Parts World

NEPAG helps to Develop/Maintain Standards for Electronic Parts



The parts users and standards organizations work with suppliers to ensure availability of standard parts for NASA, DoD and others. **For Space microcircuits, DLA, NASA (S. Agarwal) and the U.S. Air Force / Aerospace Corp. (L. Harzstark) form the Qualifying Activity (QA).**

MIL-STD-883, Test Method 1005

MIL-STD-883J
w/CHANGE 1

TABLE I. Steady-state time temperature regression. 1/ 2/ 3/ 4/

Minimum temperature T_A (°C)	Minimum time (hours)			Test condition (see 3.5)
	Class level S	Class level B	Class level S hybrids (Class K)	
100		7500	7500	Hybrid only
105		4500	4500	"
110		3000	3000	"
115		2000	2000	"
120		1500	1500	"
125	1000	1000	1000	A -E
130	900	704	—	"
135	800	496	—	"
140	700	352	—	"
145	600	256	—	"
150	500	184	—	"
175		40	—	F
180		32	—	"
185		31	—	"
190		30	—	"

1/ Test condition F shall be authorized prior to use and consists of temperatures 175°C and higher.
2/ For condition F the maximum junction temperature is unlimited and care shall be taken to ensure the device(s) does not go into thermal runaway.
3/ The only allowed conditions are as stated above.
4/ Test temperatures below 125°C may be used for hybrid circuits only.

METHOD 1005.9
26 February 2010

- Life test below 125C not allowed for monolithic microcircuits.

MIL-PRF-38535, Revision K

MIL-PRF-38535K

TABLE IA. Screening procedure for hermetic classes Q, V and non-hermetic class Y microcircuits.

Screening Tests	MIL-STD-883, test method (TM) and conditions		
	Class Q (class level B)	Class V (class level S)	Class Y (class level S)
1. Wafer lot acceptance test	QM plan (see H.3.2.1.4) 1/	QM plan (see H.3.2.1.4) 1/ or TM 5007 of MIL-STD-883 (all lots)	QM plan (see H.3.2.1.4) 1/ or TM 5007 of MIL-STD-883 (all lots)
2. Nondestructive bond pull (NDBP) test 2/		TM 2023	TM 2023
3. Internal visual inspection 3/	TM 2010, condition B	TM 2010, condition A	TM 2010, condition A
4. Temperature cycling 4/	TM 1010, condition C, 10 cycles minimum	TM 1010, condition C, 10 cycles minimum	TM 1010, condition C, 10 cycles minimum
5. Constant acceleration 5/	TM 2001, condition E (minimum), Y1 orientation only	TM 2001, condition E (minimum), Y1 orientation only	TM 2001, condition E (minimum), Y1 orientation only
6. Visual inspection 6/	100%	100%	100%
7. Particle Impact Noise Detection (PIND) test 7/ 8/		TM 2020, test condition A on each device	TM 2020, test condition A on each device
8. Serialization 9/	In accordance with device specification (100%)	In accordance with device specification (100%)	In accordance with device specification (100%)
9. Pre burn-in (interim) electrical parameters test 10/	In accordance with device specification 11/	In accordance with device specification 12/	In accordance with device specification 12/
10. Burn-in test: 10/ 13/ 14/	TM 1015 160 hours at +125°C minimum	TM 1015 240 hours at 125°C, condition D 15/	TM 1015 240 hours at 125°C , condition D 15/
11. Post burn-in (interim) electrical parameters test 10/		In accordance with device specification 12/	In accordance with device specification 12/
12. Reverse bias burn-in test (Static burn-in) 13/ 14/ 16/		TM 1015, Condition A or C; 144 hours at +125°C or 72 hours at +150°C minimum	TM 1015, Condition A or C; 144 hours at +125°C or 72 hours at +150°C minimum
13. Post burn-in (interim-reverse bias) electrical parameters test 10/		In accordance with device specification 12/	In accordance with device specification 12/

- Step 12 now includes option for static burn-in

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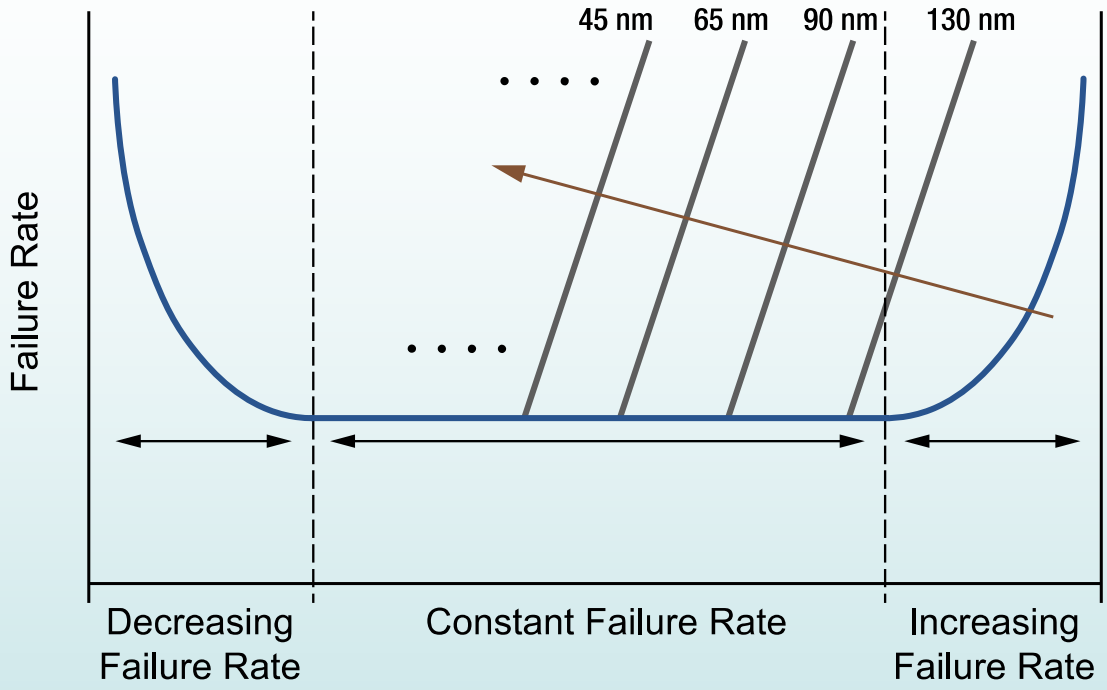
Bathtub Curve and Feature Sizes



It has been reported that as the feature sizes get smaller, the product useful life gets shorter. This should be further investigated if considering use of COTS with small features, particularly below 45nm (e.g., 35nm, 28nm, 20nm, 14nm).

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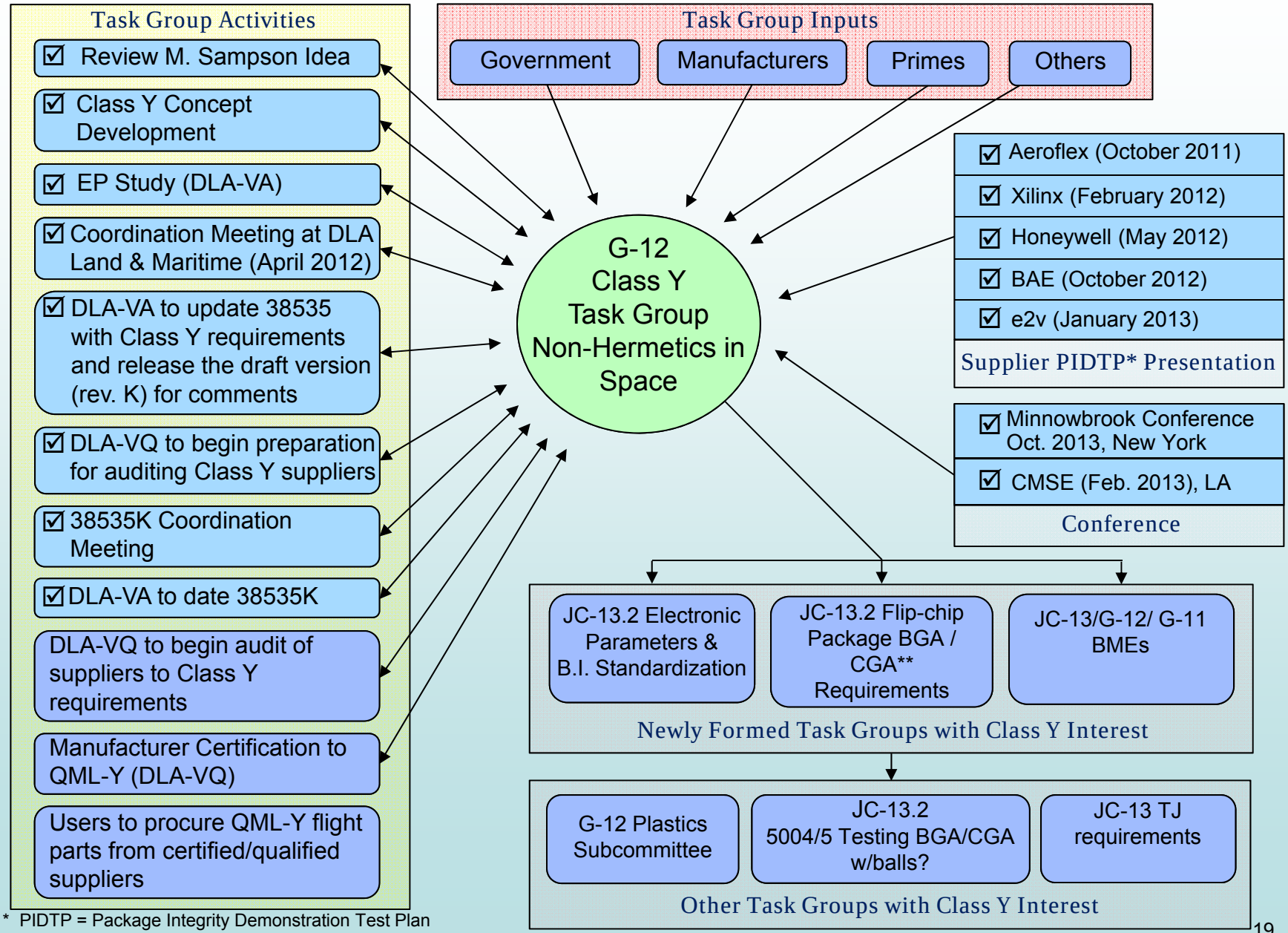
Infusion of New Technology into the QML System
G12 Class Y Effort at a Glance (e.g. Xilinx V4/V5 FPGAs)



* PIDTP = Package Integrity Demonstration Test Plan
** BGA / CGA = ball-grid array / column-grid array

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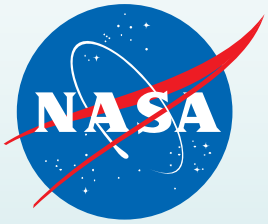
http://nepp.nasa.gov



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